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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,646	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,13,15,26-28,30 and 36-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,13,15,26-28,30 and 36-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Amendment filed February 28, 2006.

Accordingly, claims 1-3 and 11 were amended, claims 10, 12, 14, 16-25, 29 and 31-35 were cancelled, and new claims 39-50 were added. Currently, claims 1-9, 11, 13, 15, 26-28, 30 and 36-50 are pending in this application.

Allowable Subject Matter

2. The indicated allowability of claims 3, 6, 9, 28 and 38 is withdrawn in view of the newly discovered reference(s) US 5,767,531 to Yoshinouchi. Rejections based on the newly cited reference(s) follow.

The indicated allowability of claims 11, 13, 15 and 30 is also withdrawn due to double patenting rejection over copending application 09/797,186 (US 2002/0000551 A1).

Claim Objections

3. Claim 15 is objected to because of the following informalities: claim 15 claims the same subject as claim 13. Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 11, 13, 15 and 30 are provisionally rejected on the ground of nonstatutory double patenting over claims 8, 49, 50 and 52-55 of copending Application No. 09/797,186 (US 2002/0000551 A1) as shown below. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

Claims of Instant Application	Claims of Copending Application
11	8
13, 15	49, 50
30	52-55

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

An electronic equipment (of the instant application) or a semiconductor display device (of the copending application) comprising:

a pixel TFT and a driver circuit TFT, each having a semiconductor layer formed on an insulating surface, a gate insulating film formed over said semiconductor layer, a

first gate electrode comprising a first conductive film formed over said gate insulating film, and a second gate electrode comprising a second conductive film formed over said first gate electrode,

wherein said semiconductor layer of said pixel TFT comprises:

a channel forming region overlapping with said second conductive film with said gate insulating film interposed therebetween;

a first LDD region contacting said channel forming region and overlapping with said first conductive film with said gate insulating film interposed therebetween;

a second LDD region contacting said first LDD region;

a source region and/or a drain region contacting said second LDD region, and

wherein said semiconductor layer of said driver circuit TFT comprises:

a channel forming region overlapping with said second conductive film with said gate insulating film interposed therebetween;

a third LDD region contacting said channel forming region and entirely overlapping with said first conductive film with said gate insulating film interposed therebetween;

a source region and/or a drain region contacting said third LDD region, and

wherein said first conductive film has a tapered shape in cross section at an edge portion, and

wherein the width of said first conductive film in the longitudinal direction of the channel forming region is larger than that of said second conductive film.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4, 5, 7, 8, 26, 27, 39, 40, 42, 43, 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-148685 (JP'685) in view of Yoshinouchi (US 5,767,531).

Re claims 1 and 39, as shown in Fig. 1, JP'685 discloses a liquid crystal display (LCD) device (an electronic equipment) comprising:

a substrate 1 having an insulating surface (paragraph 18);

a semiconductor layer 2 (polycrystalline silicon active layer) formed over the substrate 1, said semiconductor layer having a channel forming region 7c, an LDD region 7b (low charge concentration), a source region and a drain region 7a (high charge concentration) (paragraphs 18 and 20);

a gate insulating film 3 formed on said semiconductor layer (paragraph 19);

a first gate electrode comprising a first conductive film 4 formed over said gate insulating film 3 (paragraph 19);

a second gate electrode comprising a second conductive film 5 formed over said first gate electrode (paragraph 19),

wherein the width of said first conductive film 4 in the longitudinal direction of said channel forming region 7c is larger than that of said second conductive film 5 (Fig. 1 and paragraph 19); and

wherein said LDD region 7b entirely overlaps with said first conductive film 4 with said gate insulating film 3 interposed therebetween and contacts said source region and said drain region 7a (Fig. 1 and paragraph 20).

Re claims 2 and 40, as shown in Fig. 1, JP'685 discloses a liquid crystal display (LCD) device (an electronic equipment) comprising:

a substrate 1 having an insulating surface (paragraph 18);

a semiconductor layer 2 (polycrystalline silicon active layer) formed over the substrate 1, said semiconductor layer having a channel forming region 7c, an LDD region 7b (low charge concentration), a source region and a drain region 7a (high charge concentration) (paragraphs 18 and 20);

a gate insulating film 3 formed on said semiconductor layer (paragraph 19);

a first gate electrode comprising a first conductive film 4 formed over said gate insulating film 3 (paragraph 19);

a second gate electrode comprising a second conductive film 5 formed over said first gate electrode (paragraph 19),

wherein the width of said first conductive film 4 in the longitudinal direction of said channel forming region 7c is larger than that of said second conductive film 5 (Fig. 1 and paragraph 19);

wherein said LDD region 7b entirely overlaps with said first conductive film 4 with said gate insulating film 3 interposed therebetween and contacts said source region and said drain region 7a (Fig. 1 and paragraph 20); and

wherein said channel forming region 7c between the LDD region 7b overlaps with said second conductive film 5 with said gate insulating film 3 interposed therebetween as shown in Fig. 1 (paragraph 20).

JP'685 discloses all aspects of the instant invention recited in claims 1, 2, 39 and 40 except for the gate insulating film having a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode and the second thickness is thinner than the first thickness.

As shown in Fig. 1, Yoshinouchi discloses a thin-film transistor including a semiconductor layer 3 having a source region 5a and a drain region 5b, a gate insulating film 30 (6a, 6b) formed on the semiconductor layer 3, and a gate electrode 8 formed on the gate insulating film, wherein the gate insulating film 30 has a first thickness d2 in a region where the gate insulating film 30(6b) is covered by the gate electrode 8 and a second thickness d1 including in a region where the gate insulating film 30(6a) is not covered by the gate electrode 8 and the second thickness d1 is thinner than the first thickness d2 (see Abstract and col. 6, lines 9-28).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of JP'685 with the teaching of Yoshinouchi by forming the gate insulating film having a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode and the second thickness is thinner than the first thickness in order to reduce the off current of the thin-film transistor and enhance the ability to retain a displayed image, and hence to improve the quality and reliability of the display (col. 4, line 66 through col. 5, line 13).

Re claims 4, 5, 7, 8, 42 and 43, as shown in Fig. 1, JP'685 discloses an LDD structure manufactured by ion implantation where a concentration of impurity element gradient at a portion 7b is $1x10^{17}$ atoms/cm^3 (low concentration as LDD region) and a concentration of impurity element gradient at a portion 7a is (5 to 100) $x10^{19}$ atoms/cm^3 (high concentration as source and drain regions), wherein a gate wiring structure 4, 5 is used as a mask to make the charge distribution in a self-aligning manner and a portion 7c under the gate wiring structure 4, 5 (as channel forming region 7c) is not implanted with ion (paragraphs 16 and 20). Accordingly, the concentration of said impurity element gradient increases as the distance from said channel forming region 7c (to said source and drain regions 7a) increasing.

Re claims 26, 27, 48 and 49, JP'685 discloses that the liquid crystal devices using the LDD technique are widely used for a liquid crystal television, OA equipment and the like (paragraph 7). Thus, it would have been obvious to one having ordinary skill in the art that the semiconductor device of JP'685 is applicable to electronic equipment

such as video camera, digital camera, projector, head mounted display, game apparatus, car navigation system, personal computer and portable information terminal for intended use.

8. Claims 3, 6, 9, 28, 41, 44 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-148685 (JP'685) in view of Yoshinouchi (US 5,767,531) and Nishimura et al. (Nishimura, US 6,462,802 B1).

Re claims 3 and 41, as shown in Fig. 1, JP'685 discloses a liquid crystal display (LCD) device (an electronic equipment) comprising:

a substrate 1 having an insulating surface (paragraph 18);

a semiconductor layer 2 (polycrystalline silicon active layer) formed over the substrate 1, said semiconductor layer having a channel forming region 7c, an LDD region 7b (low charge concentration), a source region and a drain region 7a (high charge concentration) (paragraphs 18 and 20);

a gate insulating film 3 formed on said semiconductor layer (paragraph 19);

a first gate electrode comprising a first conductive film 4 formed over said gate insulating film 3 (paragraph 19);

a second gate electrode comprising a second conductive film 5 formed over said first gate electrode (paragraph 19),

wherein the width of said first conductive film 4 in the longitudinal direction of said channel forming region 7c is larger than that of said second conductive film 5 (Fig. 1 and paragraph 19);

wherein said LDD region 7b entirely overlaps with said first conductive film 4 with said gate insulating film 3 interposed therebetween and contacts said source region and said drain region 7a (Fig. 1 and paragraph 20).

However, JP'685 does not disclose that the gate insulating film has a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode and the second thickness is thinner than the first thickness; and that the first conductive film has a tapered shape in cross section at an edge portion as recited in claims 3 and 41.

At first, as shown in Fig. 1, Yoshinouchi discloses a thin-film transistor including a semiconductor layer 3 having a source region 5a and a drain region 5b, a gate insulating film 30(6a, 6b) formed on the semiconductor layer 3, and a gate electrode 8 formed on the gate insulating film, wherein the gate insulating film 30 has a first thickness d2 in a region where the gate insulating film 30(6b) is covered by the gate electrode 8 and a second thickness d1 including in a region where the gate insulating film 30(6a) is not covered by the gate electrode 8 and the second thickness d1 is thinner than the first thickness d2 (see Abstract and col. 6, lines 9-28).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of JP'685 with the teaching of Yoshinouchi by forming the gate insulating film having a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode and the

second thickness is thinner than the first thickness in order to reduce the off current of the thin-film transistor and enhance the ability to retain a displayed image, and hence to improve the quality and reliability of the display (col. 4, line 66 through col. 5, line 13).

Further, as shown in Fig. 1, Nishimura discloses a liquid crystal display device comprising a gate electrode wiring 201 having a first gate electrode 107 and a second gate electrode 108 formed over said first gate electrode 107, wherein the gate electrode has a tapered shape in cross section at an edge portion to ensure a good peripheral portion around the interlayer insulating film 110 and drain electrode wiring 203 (see also Fig. 26D and col. 11, lines 39-59).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the semiconductor device of JP'685 with the teaching of Nishimura by forming a gate electrode wiring including a first conductive film of a first gate electrode having a tapered shape in cross section at an edge portion in order to prevent short circuit between wirings through the interlayer insulating film and a breakage of a drain line (col. 11, lines 52-59).

Re claims 6, 9 and 44, as shown in Fig. 1, JP'685 discloses an LDD structure manufactured by ion implantation where a concentration of impurity element gradient at a portion 7b is $1x10^{17}$ atoms/cm^3 (low concentration as LDD region) and a concentration of impurity element gradient at a portion 7a is (5 to 100) $x10^{19}$ atoms/cm^3 (high concentration as source and drain regions), wherein a gate wiring structure 4, 5 is used as a mask to make the charge distribution in a self-aligning manner and a portion 7c under the gate wiring structure 4, 5 (as channel forming region 7c) is not implanted with

ion (paragraphs 16 and 20). Accordingly, the concentration of said impurity element gradient increases as the distance from said channel forming region 7c (to said source and drain regions 7a) increasing.

Re claims 28 and 50, JP'685 discloses that the liquid crystal devices using the LDD technique are widely used for a liquid crystal television, OA equipment and the like (paragraph 7). Thus, it would have been obvious to one having ordinary skill in the art that the LCD device of JP'685 is applicable to electronic equipment such as video camera, digital camera, projector, head mounted display, game apparatus, car navigation system, personal computer and portable information terminal for intended use.

9. Claims 36, 37, 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-148685 (JP'685) in view of Yoshinouchi (US 5,767,531) as applied to claims 1, 2, 4, 5, 7, 8, 26, 27, 39, 40, 42, 43, 48 and 49 above, and further in view of Hirataka et al. (Hirataka, USPN 5,982,471).

The LCD device of JP'685 as modified in view of Yoshinouchi includes all that is recited in claims 36, 37, 45 and 46 except for an organic interlayer insulating film formed over the first and second gate electrodes.

As shown in Figs. 5F and 5G, Hirataka discloses an insulating film 319 formed over a gate electrode 305, wherein the insulating film comprises an organic insulating material (col. 10, lines 19-27).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the LCD device of JP'685 with the

teaching of Hirataka by forming an interlayer insulating film over the first and second gate electrodes, wherein the interlayer insulating film comprises an organic insulating material in order to planarize the surface of the interlayer insulating film and make the cell gap uniform (col. 10, lines 23-25).

10. Claims 38 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-148685 (JP'685) in view of Yoshinouchi (US 5,767,531) and Nishimura et al. (Nishimura, US 6,462,802 B1) as applied to claims 3, 6, 9, 28, 41, 44 and 50 above, and further in view of Hirataka et al. (Hirataka, USPN 5,982,471).

The LCD device of JP'685 as modified in view of Yoshinouchi and Nishimura includes all that is recited in claims 38 and 47 except for an organic interlayer insulating film formed over the first and second gate electrodes.

As shown in Figs. 5F and 5G, Hirataka discloses an insulating film 319 formed over a gate electrode 305, wherein the insulating film comprises an organic insulating material (col. 10, lines 19-27).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the semiconductor device of JP'685 with the teaching of Hirataka by forming an interlayer insulating film over the first and second gate electrodes, wherein the interlayer insulating film comprises an organic insulating material in order to planarize the surface of the interlayer insulating film and make the cell gap uniform (col. 10, lines 23-25).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached at (571) 272-1787.

Thoi V. Duong 

05/03/2006